**ELEC2205 Electronic Design**

**D4 System Design Exercise 2015**

**SPECIES:**

**a Secure & Portable Electronic Communication Invention  
to Ensure human Survival**

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# Introduction

Your job, working as a design consultancy formed of 5-6 students, is to design and build a new secure and mobile communication system in 12 days. You will be competing with 10 other teams to design the best product.

## Background

“3 billion human lives ended on August 29th, 1997. The survivors of the nuclear fire called the war Judgment Day. They lived only to face a new nightmare, the war against the Machines...”

*Prologue from “Terminator 2,” Tri-Star Pictures, 1991*

Ok, so 1997 came and went without disaster. But assume for a second that it hadn’t – the scenario for D4 2015 is based on this proviso. The year is now 1998, and humankind are having trouble communicating with one another over reasonably short distances of tens of meters – they need to be able to do this both to coordinate their ‘*war against the machines*’, and also to stay safe (so people can move around without being spotted).

Your design consultancy, along with 10 others, have been tasked (by humanity) with designing a portable system to help the surviving humans to communicate with each other to avoid extinction by robots and to rebuild the world. The robots aren’t stupid – after all, their intelligence is supposed to have exceeded that of human’s (the ‘singularity’) – so ensuring secure communication is essential. Due to the wonders of time travel (luckily this is completely feasible within the Terminator 2 scenario), your team is able to leverage 2015 technology to design and develop a prototype of this portable and secure communication system.

At the end of the exercise, your team will present and demonstrate your prototype system to a panel of judges, who will pick the system that everyone will put their faith in to save humankind… So no pressure!

## Requirements

Your design should comprise all of the following:

**User Input** – Essential for useful communication, your system needs some way of capturing user input to communicate. In the case of a typical mobile phone, this is a keypad, microphone, camera etc. Your system MUST be capable of capturing human voice (with a minimum bandwidth of 4 kHz). However, you are encouraged to supplement this with other inputs (e.g. a camera, keypad, or other sensors – perhaps you could detect hand gestures!) if you wish.

**User Output** – You MUST have at least one method of presenting the received communication to the user. In the case of a typical mobile phone, this is via the display screen, speaker etc. There are no constraints on how you output communicated data, other than it should be effective. You may wish to use a speaker (in which case you should also think about appropriate amplification), LCD, tactile feedback, etc.

**Security** – you MUST ensure that communication is secure (e.g. stopping the communication being eavesdropped or maliciously modified). Can you provide authentication so that you know the person you’re communicating with is who they say they are?

**Resilience –** it is highly likely that other team will be trying to communicate using the same frequency and/or radio modules as you. You MUST ensure that you are able to operate in the presence of interference, and that other communications are able to occur simultaneously (i.e. ‘shouting the loudest’ and blocking all other RF is not an acceptable solution!)

**Wireless communication** – Your device MUST be capable of real-time, low-latency, short range (10s of metres, indoors) wireless communication to a second device. You MUST prototype at least two communication devices in order to demonstrate this!

**Power management** – Your system MUST be portable, and hence is likely to be battery operated. The power consumption of the system must be managed, so that it can continue operating for extended periods without requiring excessively heavy batteries. Can you incorporate low-power into your design process? How will you test its power consumption? How long will it be able to operate off batteries? How do you consider the balance between size/weight and battery life?

You are encouraged to also include any other additional features that you like. The robots are a pretty advanced ‘species’ after all, and humankind need some special features if they’re to have the upper edge. The following are some ideas and examples only – you are encouraged to be creative:

**Additional handsets –** Can you demonstrate an ability to address a particular device you want to communicate with (by addressing it, e.g. a phone number in a typical mobile phone). You may want to think of other ways of addressing other devices, for example geographical. Can multiple calls be made at the same time (e.g. handset A -> handset B at the same time as handset C -> handset D)? Perhaps you wish to support multicast (communicating with multiple devices at the same time)? Of course, for all of these you will probably need to prototype more than two devices!

**Compression** – you may decide to compress your communication, e.g. to increase the quality of communicated data.

**Adaptive audio capture** – Your system is likely to operate in a variety of different scenarios, for example whispered voices in quiet environments to shouting in very noisy environments.

**Speakerphone** – to enable received communication to be presented to larger audiences.

**Ringtones and notifications** – How does the receiver know when you want to communicate with them? A ringtone may be one option, but might this create problems in the target environment (it’s bad enough when someone’s phone goes off in a lecture!). Perhaps you can think of other ways to notify the receiver.

**Appearance, mechanical operation, ruggedisation** – Your system is supposed to be portable, and hence you could choose to house your electronics in a box to stop them from getting damaged easily. You may like to think about shower-proofing for the extreme environments that it is supposed to operate in.

**Peer to Peer communication** – Can you support communication over longer distances by supporting peer-to-peer networking (i.e. routing communication across intermediate devices). Perhaps you could support voice communication only over direct links, but provide support for other low-data-rate transfers (e.g. text-based messages) in this way? Of course, to demonstrate and evaluate peer-to-peer operation, you will need to make more than two devices!

**Hands free operation** – can you support hands free operation, perhaps using a standard wired headset (with a 3.5mm jack socket), a Bluetooth headset, or something completely new and creative!?

**Storage** – The device could record and store communications so that they can be later replayed. For example, you could use standard media (such as SD card) for later playback on a PC or on the device itself.

## Research

It would be great to see a wide variety of different system designs among the different teams. You and your team should spend some time brainstorming ideas, rather than jumping on the first idea that springs to mind. You may like to combine the best parts of the various ideas that you come up with. There are lots of places you can look for ideas:

* Literature (you should include some good references in your final report), e.g.   
  <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=1589644>
* Hobby websites, e.g. <http://hackaday.com/category/radio-hacks/>, <http://hackaday.com/?s=communication>, etc

## Overview

The exercise has been developed to reflect commercial practice as far as possible, testing and assessing your abilities at a variety of skills, such as:

* working in groups and partitioning a large task amongst individuals;
* creativity and innovation;
* mixed-signal electronic design;
* initiative;
* costing and budgeting;
* time management;
* troubleshooting;
* technical research.

The assessment contributes approximately 50% of the ELEC2205 module, or equivalently 7.5 credits. As such each team member is expected to put in 75 hours of work in undertaking the design, development and reporting.

The exercise takes place over a four week period, with the following structure:

1. Design, investigation and simulation.
2. Prototyping and construction.
3. Final assembly, evaluation and report production.
4. Trade fair

The trade fair on 20th March is a competitive event, and a prize will be awarded to the team that impresses the judges the most with their design, presentation and demonstration/performance. BAE Systems Applied Intelligence ESG sponsors the prize[[1]](#footnote-1) and the judging panel will consist of Simon Jupp (BAE Systems Applied Intelligence) and Tim Forcer (ECS). Each member of the winning team will receive a £100 Amazon voucher. The winners will be announced at the trade fair on the afternoon of 20th March.

This is a team project, and a substantial number of the marks are for the team report and team design. However, all team members are expected to make an individual contribution to the team, and you will be assessed on this basis as well. Therefore, while it is okay for you to work on a subsystem in a pair, you must be able to clearly explain your contribution to that subsystem, and to the project as a whole.

## Evaluation

Your marks for the D4 exercise are based on your technical solution, design process, team dynamics, the report that you submit, and your team’s presentation at the trade fair. In evaluating your work the following points will be considered:

* Difficulty of the problem addressed
* Electronic design
* Ease of use of the device
* Creativity and innovation
* Aesthetics
* Cost
* Reliability
* Documentation

## Acknowledgements

The authors gratefully acknowledge the support of David Oakley, Jeff Hooker, David Kemmish, Mark Temple, Tim Forcer and Simon Jupp in preparing for this exercise. The remainder of this document describes the requirements of the project, the logistics, the resources available and the deliverables.

# Specification

Your team is a small electronic design consultancy, which has been tasked (by humanity) to design and prototype a portable and secure system which can be used to communicate over short distances (10s of metres). You have 12 working days to design and build a working prototype. So that it doesn’t put ‘[*all its eggs in one basket*](http://dictionary.cambridge.org/dictionary/british/put-all-your-eggs-in-one-basket)’, humanity has also contacted some other design consultancies to produce competing designs. You will market your product at a trade fair, and will be judged by a panel of judges. In proposing your design, you must decide on what you think is achievable with the time and resources available.

## Design Decisions

There are always many different ways to solve a design problem. However, the most robust and elegant solutions are usually the simplest. Always ask the question: “Is there a simpler way?” Consider carefully what is best done in hardware, and what in software. You should give thought to the complexities, practicalities, suitability and benefits of all the options. Remember a stripped down system that works will be better than a more complex one that fails. Try to mitigate the risk of a failed design by concentrating on the central elements and enabling features to be scaled up when the critical part is working. Remember that components that you have used before are less likely to reveal unexpected behaviour.

Although you have lots of experience using the AVR and it is quite a powerful computer, it does have limitations; it has a small internal data memory, the program memory is not generous and the clock speed is limited to 20MHz. The Stellaris and other ARM processors are a more powerful alternative. You will need to look carefully at exactly what you can and cannot do. But remember, there is no limitation on the number of chips you may use.

## Prototyping and Construction

When working with mixed-signal systems, care must be taken in separating the analogue and digital grounds to avoid interference from the digital part affecting the sensitive analogue part. More details can be found in [The Circuit Designer's Companion](http://lib.myilibrary.com/Open.aspx?id=100939)*.* Also, remember to decouple your ICs.

## Testing and Evaluation

Individual modules and milestones should be verified as you go and recorded on the design completion form of Appendix D. It is your responsibility to design tests that demonstrate and validate the capabilities of your design.

Results and testing are a core part of the exercise, and carry significant weight in the mark scheme. Make sure that you record evidence of your progress and testing, and that you think about how to evaluate your system and its subsystems – not just ‘*does it work?*’, but also ‘*how well does it work?*’. You should also think of the process and use of testing in a number of different ways, e.g.:

1. testing as part of the design process, for example simulation and emulation;
2. testing as a way of validating that your subsystems work and as intended (e.g. bugfixing);
3. testing to understand how well the complete system works (and under what conditions it doesn’t work), compared against your original specification.

## Features

During the design phase you might like to think about how you are going to market your device at the trade fair. What is your market niche? High performance, super signal processing, low power, low cost …?

# Logistics

For this design exercise you are required to work together in a team of 5-6 students. The teams are given in Appendix C. Your team will elect a representative to be the project team leader. This team leader will be responsible for co-ordinating meetings between you all, to ensure that a successful collaborative design becomes a demonstrable reality by the end of your last day in the laboratory. You must collectively partition the work of the project evenly among the members of your team, making arrangements to ensure that the various modules of the design will interface correctly, integrating to become the overall system, and put in place a mechanism for monitoring progress and redistributing effort if part of the project is not going well. You are strongly encouraged to make use of the [ECS project management system](https://forge.ecs.soton.ac.uk/) and [ECS Source Kettle](https://devtrack.ecs.soton.ac.uk) for managing the project and maintaining source code.

## Week 0: Introduction

In week 0, you should meet with your team, allocate roles to each team member, decide on the scope of your project, research possible solutions and begin the design of these. It is a critical phase in the project since you are required to attend a design clinic on Monday 23rd February with your initial design and to place your order for components by 14:00 on Tuesday 24th February. Therefore, you must work intensively in this period and will likely need to make use of your weekend.

|  |  |  |  |
| --- | --- | --- | --- |
| Day | Time | Location | Activity |
| Thur 19/2 | 10:00-12:00 | 46/2003 | Kick-off Presentation |
| Outside Lectures |  | First Team Meeting |
| Fri 20/2 | Outside Lectures |  | Initial investigation and design |

## Week 1: Design, investigation and simulation

During the first week there will be opportunities to get feedback on your design. On Monday your team will meet with Tim Forcer to get early feedback on the design approach – please bring and hand over a sketch of how you envisage your device, a 150 word abstract describing what it does and a legible high-level block schematic, with the primary component(s) noted on each block. At the beginning of your laboratory session on Friday a member of academic staff will review your design, and will advise you as to their impression of the likelihood of success. We believe that simple designs will stand a much higher chance of success than complex ones. We will look at your design completion form and may request that you add some more detail to this.

|  |  |  |  |
| --- | --- | --- | --- |
| Day | Time | Location | Activity |
| Mon 23/2 | Outside Lectures |  | Refine initial design, and draft first versions of software (SystemVerilog, C, …)  Collect box of bits from the Zepler Lab Support Hatch |
| Appendix G | Laboratory | Design Clinic (20 minute slot per team) |
| Tue 24/2 | Outside Lectures |  | Refine design, prepare project proposal form and draft first versions of software |
| 14:00 | Zepler Lab Support Hatch | Deadline for submission of kit & component requisition form to David Kemmish/Mark Temple and ECS Electronic Handin System. |
| Wed 25/2 | Outside Lectures |  | Refine design, prepare project proposal form and draft first versions of software |
| Thur 26/2 | Outside Lectures |  | Refine design, prepare project proposal form and draft first versions of software |
| Fri 27/2 | 10:00 | Electronic Handin System | Submit project proposal form to the ECS Electronic Handin System. |
| 10:00-13:00 | Laboratory | Teams Armageddon – Halo: initial investigations in the lab. Negotiation of design completion form with Geoff, Steve or Rob. |
| 14:00-17:00 | Laboratory | Teams Independence – Terminator initial investigations in the lab. Negotiation of design completion form with Geoff, Steve or Rob. |

## Week 2: Prototyping and construction

This is the week where your team will be able to prototype and implement the majority of its design. Although only three formal lab slots are allocated for each team in the second year laboratory, the lab will be available to you outside of your scheduled lectures this week, and you are advised to use it. The table below shows the lab opening times, which enables you to be in the lab every day. It is a good idea to get incremental goals ticked off on the design completion form during the supervised slots in this week.

|  |  |  |  |
| --- | --- | --- | --- |
| Day | Time | Location | Activity |
| Mon 2/3 | 10:00-13:00 | Laboratory | Teams Armageddon – Halo prototyping in the lab with supervision |
| 14:00-17:00 | Laboratory | Teams Independence – Terminator prototyping in the lab with supervision |
| Tue 3/3 | 12:00 | Lab Support Hatch | Scheduled delivery of kit & components ordered from Onecall and RS |
| Outside lectures | Laboratory | All teams have an opportunity to work in lab without supervision, subject to the agreement of the lab support staff. |
| Wed 4/3 | Outside lectures | Laboratory |
| Thur 5/3 | Outside lectures | Laboratory |
| Fri 6/3 | 10:00-13:00 | Laboratory | All teams prototyping and assembling sub-systems in the lab with supervision |
| 14:00-17:00 | Laboratory |

By the end of this week you should aim to have the individual components of your design working, ready for the final integration on Monday.

## Week 3: Final assembly, evaluation, and report production

Monday is judgement day which sees final assembly of your prototype and its evaluation. At the end of the day before the lab closes your team must demonstrate your system to the supervising member of staff, who will finalise your Design Completion Form with details of the success or failure of any remaining aspects of your design. There will be no extension to the laboratory time allocated to your team. Your design will be signed off in whatever state it is at the end of the session. Moreover, all your team’s hardware must be handed in after marking on that day so that your team can be signed-off as “all items returned”.

|  |  |  |  |
| --- | --- | --- | --- |
| Day | Time | Location | Activity |
| Mon 9/3 | 10:00-13:00 | Laboratory | All teams completing final assembly and evaluation with supervision. You may like to capture some video footage and still imagery of your prototype(s) in action. |
| 14:00-17:00 | Laboratory |
| 16:30 |  | All construction stops |
| 17:00 |  | Deadline for finalising design completion forms, handing over your prototype(s) and returning other items to the Zepler Lab Support Hatch |
| Tue 10/3 | Outside lectures |  | Fill out the project completion form (Appendix E).  Your team should write the final report. |
| Wed 11/3 | Outside lectures |  |
| Thur 12/3 | Outside lectures |  |
| Fri 13/3 | Outside lectures |  |
| 16:00 |  | Deadline for the final report. Each member of your team should submit their individual report to the ECS Electronic Handin System. One member of your team should submit the group report to the ECS Electronic Handin System and print out the receipt. The receipt should be bound to a hard copy of your group and individual reports, which should be submitted to the Zepler reception before 4pm on Friday 13th March. |

## Week 4: Trade fair

Your hardware will be returned to you on the day of the trade fair. You must not make any further modifications or improvements to the design, but can check that it is still working as you left it.

|  |  |  |  |
| --- | --- | --- | --- |
| Day | Time | Location | Activity |
| Mon 16/3 | Outside lectures |  | Prepare trade-fair slides to detail the technical, marketing and costing aspects of your prototype. Prepare a video advert lasting no longer than one minute to showcase the features of your product to a commercial audience. |
| Tue 17/3 | Outside lectures |  |
| Wed 18/3 | Outside lectures |  |
| Thur 19/3 | Outside lectures |  |
| 16:00 | Electronic Handin System | Deadline for submitting presentation slides and advert to the ECS Electronic Handin System |
| Fri 20/3 | 10:00-13:00 | 67/1007 | All members of your team should attend the trade-fair. One member of your team should present your slides and advert. |
| 14:00-14:30 | Laboratory | One member of your team should attend to setup your hardware, ready for demonstration to the judges. |
| 14:30-17:00 | Laboratory | One member of your team should attend to demonstrate your hardware to the judges. |
| 17:00-18:00 | Laboratory | All members of your team should attend the closing ceremony. Teams with working prototypes are invited to give a quick live performance and prizes will be awarded by the judges. |

# Resources

As this exercise is about initiative, you may choose to use any technology or solutions. However, you are not allowed to use purpose built solutions, and your plan for the final delivered prototype(s) must not contain any protoboards.

## Research

In developing your design you may wish to use elements of hardware or software of other designs you may be able to find. Note that this is only acceptable provided you follow the [standard procedures for academic integrity](https://secure.ecs.soton.ac.uk/kb/entry/35/). Simply copying large parts of another design will result in a low mark for the exercise. However, re-using and referencing an element from another design because you understand it and think it is good is fine. Ultimately, the balance between your own ideas and those of others will moderate the marking of your design. Furthermore, make good use of software libraries where they exist.

## Kit & Components

To help you with the design we will provide you with a “box of bits” containing some components which may be useful[[2]](#footnote-2) (see Appendix F). You are required to submit a list of any additional items you require to David Kemmish/Mark Temple using the form in Appendix B, not later than 14:00 on Tuesday 24th February. Items you may request include:

* Altera FPGA board with cables (maximum one per team)
* [RFM12B-S2 wireless transceiver modules with breakout boards](http://www.hobbytronics.co.uk/rfm12b-wireless-breakout) (you are already given two of these in your ‘Box of Bits’ but, if desired, you should be able to request up to two more per team).
* MSP430 boards and programmers (there are limited numbers of these in stores, so there is a maximum of one per team and they will be offered on a “first come, first served” basis). We have some of [MSP-EXP430FG4618](http://www.ti.com/tool/msp-exp430fg4618), [MSP-EXP430F5529LP](http://www.ti.com/tool/msp-exp430f5529lp), [MSP-FET430UIDF](http://www.ti.com/tool/msp-fet430uif) and [EZ430-F2013](http://www.ti.com/tool/EZ430-F2013).
* Stellaris ARM processor development board (maximum one per team)
* ISP programming adaptor for PLDs (maximum one per team)
* A small number of Arduinos
* ispGAL22V10 PLDs
* FTD USB interface modules
* Photodiodes
* Anything available from the lab component drawers
* Standard components stocked by Lab Stores
* Connectors or cables that you might need for testing or to connect modules or boards together.
* SD Card reader (<https://secure.ecs.soton.ac.uk/notes/ellabs/databook/equip/SD_card_types.pdf>)
* Soldering irons, solder, solder suckers and solderwick.
* Surface mount solder stations.
* protoboards,
* DMMs
* sets of digital scope probes
* [Micro arcana kits – Il Matto, Il Bagatto, La Papessa, L'Imperatrice](https://secure.ecs.soton.ac.uk/notes/elec2032/D4/Micro%20Arcana/)
* [Accelerometers](https://www.sparkfun.com/products/11770)
* [OV7670 FIFO camera module](http://emartee.com/product/42043/OV7670%20AL422%20FIFO%20Camera%20Module) ([Source code for AVR](https://sourcekettle.ecs.soton.ac.uk/project/OV7670_Test))
* [2.2” TFT QVGA Display](https://secure.ecs.soton.ac.uk/notes/elec2032/D4/Micro%20Arcana/)

Your team has a budget of £50 for purchasing components (from [Onecall](http://onecall.farnell.com/) and/or [RS](http://uk.rs-online.com/web/)[[3]](#footnote-3)) that are not available from Lab Stores or in your Box-of-bits. You can ignore any shipping costs from these suppliers. You may also obtain components from Maplin (or anywhere else) if you wish provided: (a) you pay for them yourselves, (b) you collect them yourselves, (c) you have made a sufficiently good case for their need in your project proposal form and (d) you do not expect to get them back at the end of the project.

Bonus marks will be awarded to teams that step out of their comfort zone and use components that they have not had experience with before – being able to pick up new kit and run with it is an important skill for an Electronic Engineer. Of course, there is a risk associated with using unfamiliar equipment and so you should plan and manage your project to mitigate this.

All of the above items must be ordered in advance and must be handed back by 17:00 Monday 09th March, and signed off by a member of staff or by someone in stores. The technical staff have absolute authority to refuse your order without appeal if they are not satisfied. Should this happen you must contact Dave Oakley or Geoff Merrett (by email in the first instance) as soon as possible to rectify the matter. Please note that any self-purchased items must also be handed in, and will not be returned after the exercise. You may negotiate with technical staff about their return, after the exercise has been fully marked, in June.

Remember – Keep it Simple

A shot-gun approach, i.e. let’s have lots of everything at the beginning, is usually the sign of a poor design.

## Prototyping and Construction

Protoboard some elements first to quickly identify issues. Read the datasheets – they contain a lot of useful information. Remember, the idea is to identify any unexpected behaviour or misconceptions/complications in your design. Your plan for the device you will submit must not contain any protoboards. You may choose to construct using any of a variety of approaches such as tri-pad, strip-board, wire-wrap, or dead bug. Remember to request anything you need on the Kit & Component Requisition form (Appendix B). Think carefully about the choice of packaging of all components. If you do decide to use any surface-mount components consult with the members of your team who have been trained in basic surface-mount technology to decide on which packages are realistic to work with. We can provide some DIL adaptors for surface mount components.

## Laboratory Resources

Your team will be allocated a number of benches in the Electronics laboratory for the sole use of your team throughout the duration of the prototyping and construction phase of the exercise (27th February to 09th March). During this period there are no other Part I or Part II laboratories and you may leave materials on these benches overnight. The allocation is shown in Appendix H. When you are not scheduled into the labs on Friday 27th February and Monday 02nd March, you are still free to use any of the computing facilties in Zepler or elsewhere on campus for simulation etc.

## Costing

The development and manufacture of your design incurs many costs, which the customer hopes to recover (along with some profit!) through selling your product. Your report should include a detailed and justified breakdown of these costs. There are two types of costs:

1. Fixed costs, which do not depend on how many units you build. These include:

* Hardware and software development costs. Your report should specify how many person-hours your team spent on D4 up until the prototype was handed over. Each of these person-hours incurs a cost of £75.
* Development component costs. Your report should include a detailed costing of all the components you acquired for D4 (whether you used them or not), including any items from the box of bits. Use Onecall or RS websites to obtain prices; you should **\*not\*** use quantity discount figures from these sites where available for the development cost. You should not include the cost of PCs, bench power supplies, test equipment and device programmers; these are all accounted for in the depreciation part of the manufacture overheads.
* Conformance testing, to obtain a CE mark. This is £2000.
* Development and manufacture overheads incurred, including rent, service bills, depreciation, repair of equipment, etc. This incurs a cost of £100k.

1. Variable costs, which are proportional to the number of units you build. These include:

* Manufacture component costs. Your report should include a detailed costing of all components required to build your product, including any items from the box of bits. Use Onecall or RS websites to obtain prices; you may use quantity discount figures from these sites where available for the manufacture cost. You should not include the cost of PCs, bench power supplies, test equipment and device programmers. These are all accounted for in the depreciation part of the manufacture overheads.
* Assembly costs. Your report should include a detailed and justified estimate of how many person-hours it would take to assemble each unit on a production line. This should include the time it takes to collect the components, solder them together, flash the ROMs, manually adjust the trimmers, house the components in a case, package the completed unit, etc. You pay your skilled work force £10 per hour.

Your report should specify and justify a recommended retail price for your product, excluding shipping, but including VAT at 20%. You should state how many units will need to be built and sold (considering a less than 100% production yield) for you to turn a profit.

# Deliverables

You will be assessed by a number of deliverables. The weighting of the deliverables is approximately:

5/100 Project Proposal Form,

15/100 Constructed Prototype & Design Completion Form,

5/100 Project Presentation,

10/100 Team Report,

65/100 Individual Report (detailed below)

The weighting of marks for the individual Report is approximately:

20/65 Technical Approach

15/65 Achievement and Results

10/65 Reporting Writing and Structure

10/65 Team Working, Planning and Progress

10/65 Evaluation and Reflection

At the end of the project, your team will have to agree on the effort contributed by each team member. This will be used as an indication of how team marks should be allocated across the team.

## Project Proposal Form

The environment of the design exercise is supposed to reflect commercial practice as far is possible. For this reason, your team will be required to submit a completed Project Proposal Form (you may edit the electronic version from appendix A). This form requires you to explain in broad terms what your proposed designs are, for both the hardware and the software, and to provide cost estimates for producing your prototype implementation. These estimates will include software development and manpower estimates. A percentage of the mark is allocated to the proposal form. Failure to submit this form by the deadline will automatically disqualify each member of the team from receiving that portion of the marks.

The project proposal form consists of four items:

1. A copy of the form from Appendix A, with the responsibilities/overall design summary, multiple module design proposals (there should be one for each module of the whole project), the cost estimates, the prototyping/construction and the planned activities sections.
2. An annotated circuit diagram of all the circuitry you expect to build (output from a CAD application or diagramming application is preferable, otherwise neat hand-drawn diagrams are acceptable provided they are scanned in for electronic submission). Depending on the state of your design process, you may choose to supply full schematics or block schematics or a mixture. This diagram should identify which communication protocols are to be used to interface between blocks.
3. Initial listings of any software (C, SystemVerilog, …); these do not have to be fully functional, but software should compile correctly and circuits should make sense. This is not just a bureaucratic requirement. Experience has shown that to finish the design exercise you must start construction of the software and circuitry early in order to have time for debugging, integration and testing. Pseudo-code is acceptable where algorithms and high-level structuring are being defined.
4. An edited Design completion form from Appendix D specifying 10-15 milestones in your project which can be signed off as you progress.

The project proposal form is to be submitted electronically to the hand-in system by 10:00 Friday 27th February. Additionally, you should bring a paper copy of all items to your laboratory session on Friday 27th February.

## Constructed Prototype

You are required to produce a working prototype of your design. During development you are able to get working elements verified and recorded on the design completion form by a supervisor. The final prototype must be handed over no later than 17:00 Monday 09th March and should contain no protoboards.

## Project Presentation

You are required to give a six minute presentation of your final design at the Trade-Fair on the 20th March, to the customer and your classmates. Your presentation will start with a video advert (duration 60 seconds) and be followed by a series of presentation slides to advertise your prototype (max duration 5 minutes).

* Your advert should be a standalone file that will play in [VLC](http://www.videolan.org/vlc/). You may also like to try embedding the advert into your presentation, but experience shows that this doesn’t always work properly. Your advert is played first, so sets the scene for your presentation. The advert is your marketing campaign, so it should encompass the key features of your product, and show it working (or at least, everything that it was able to do!). You should also try and make it engaging, as you want people to remember it. Don’t forget to capture some material (e.g. images, video, audio) during your scheduled lab time on Monday 9th March – after this point, you will not be able to access your system until the afternoon of the Trade Fair!
* Your presentation is your opportunity to pitch your product/system to the judges. Consider it like a Dragon’s Den presentation – you are trying to get the judges to understand and support your product. Your presentation slides should describe the problem you solved, your target market, the costing of your device, your design, the problems you encountered and the performance of the final prototype. Do not try to put in too much material and compensate by talking like [John Moschitta](http://en.wikipedia.org/wiki/John_Moschitta,_Jr.); practice the talk and time it; think how you might make it stand-out from the others.

Please make sure that you consider your audience: both your course mates and judges (including representatives from industry). An entertaining presentation/advert is fine, but remember that you will be pitching to a potential future employer(s). Please also make sure that your presentation and advert are sensitive to and respect the cultures, backgrounds, feelings and beliefs of others.

An electronic copy of your slides and advert should be submitted to the ECS Electronic Handin System by 16:00, 19th March. You should include no more than 10 slides and these should be contained in a single ppt, pptx or pdf file. Your files will be transferred onto the presentation computer. The whole team must attend the trade-fair, but one team member must be elected to give the presentation.

## Team Project Report

The team report should be edited by all members of the team to summarise the overall design, system integration, team working practices and costing/marketing aspects. The report should follow the following structure:

* 1. Challenge Solution Statement (*this section is based on what the* ***aims*** *were*)
* Describe the specific challenge(s) that your Solution Concept addresses
* What is the specification that your team chose at the start of the design process?
* Be ***specific***, it’s a ***specific***ation.
  1. System Design (*this section is based on what your team* ***designed***)
* Explain the design of your system, at a high level.
* Include a block diagram showing all of the subsystems and how they are connected.
* Why did you choose this particular architecture? What other options did you consider?
  1. Design Evaluation (*this section is based on what your team* ***designed***)
* How did your design match up against the criteria of 1) difficulty of the specification attempted, 2) quality of the electronic design, 3) ease of use, 4) creativity and innovation of the designed product, 5) aesthetics, 6) cost, and 7) reliability?
* You should evaluate it against each of these criteria, in separate paragraphs, followed by any additional criteria that you wish to include.
  1. Costing, Marketing and Conformance marking
* Provide details of each of these aspects.
  1. Final Product (*this section is based on what was* ***actually*** *produced*)
* Be critical, and compare your achievements against your specification
* Include a photo(s) of the final product, and an explanation of how it works
* Discuss further extensions that could be made.

References

Appendix A: Design Completion Form

* You should scan in your signed Design Completion Form (Appendix D) and include it here.

Appendix B: Project Completion Form

* You should complete the Project Completion Form (Appendix E) and include it here.

Appendix C: Circuit Diagrams

* The report should include complete circuit schematics, drawn consistently using hierarchical structures and block diagram linking.

Appendix D: Software Listings

* Include listings of your software, clearly identified and complete with line numbers.

Appendix E: Project Meeting Agendas & Minutes

* Include records of the agendas and minutes from all your project meetings.

Each section can be up to 600 words long, and hence a maximum word count of 3000 words if all sections are fully populated; figures, diagrams, tables and appendices are not included in this count. The team report should contain only things that don’t make sense to include in one of the individual reports. If a module was developed by a particular team member, then it should be discussed in the corresponding individual report. However, the team report may discuss its interface with another team member’s module, for example.

There are no mandated formatting templates or requirements for the reports, but they should be formatted in a single-column (do not use the double-column template used in the first year A10/A12 assignments). However, we would recommend using something similar to the formatting and layout used in the ‘Technical Report’ example on <https://secure.ecs.soton.ac.uk/support/textools/templates/>). For those using LaTeX, document templates are available on this page too. If you are using Microsoft Word, you may want to investigate the Master Documents and Subdocuments feature, in order to coordinate a group report.

## Individual Report

Each member of the team is also required to submit an individual report focussing on their contributions to the project and reflecting on the project as a whole. The report should follow the following structure:

* + 1. Contribution

- Identify exactly what you were tasked to do, and what you did.

* + 1. Specification
       - What were *you* trying to design?
       - What were the specified design targets for your subsystem(s)?
       - Be **specific**, it’s a **specific**ation – e.g. the specification of the audio amplifier was: a gain of *x*, a bandwidth of *y*, capable of amplifying two independent audio channels, etc.
    2. Design & Simulation
       - Describe in detail the parts that you were responsible for.
       - How did you design them?
       - Include any simulation results, or any other testing you did at the design stage
    3. Testing & Results
       - Detail the testing that you undertook on your modules.
       - Discuss the testing of each module’s interface with the rest of the system.
       - Results and testing are a core part of the exercise, and carry significant weight in the mark scheme. It should not only include ‘does it work?’, but also ‘how well does it work?’
    4. Management/Team Working
       - If you were not the team leader: you should explain how you planned and managed your own contribution to the project, and *reflect* on how the team was managed.
       - If you were the team leader: you should also include a description and reflection on your approach to managing the team, what methods you used, and how you overcame conflicts and problems, etc.
       - Describe any management roles and team working practices
       - How did your team decide to partition the work?
       - How did you and your team plan the project and its subsystems?
       - What tactics did your team employ for group working?
       - How did you and your team manage risks and respond to unexpected events?
    5. Critical Evaluation & Reflection
       - A candid description of what worked and what failed.
       - This is not an explanation of what your product did and didn’t do at the end of the project. It is an evaluation and reflection on the project as a whole, e.g. team working, your contribution, your technical contribution, etc. You should be trying to identify the weaknesses and criticisms of your work – before the examiner does!

Appendix A: …

* + - * Use appendices as required

The individual report has a maximum word count of 3000 words and it is expected that the majority of this will be in sections 3 and 4; figures, diagrams, tables and appendices are not included in this count. You do not need to duplicate material from the appendices in the team report – simply make a reference to it. Your report should acknowledge all sources in the reference section.

A zip file containing copies of all software and CAD files (C, SystemVerilog, schematics, etc), source files and binary executable must be submitted via the hand-in system along with the report.

Listings should be printed with line numbers, in a non-proportional font, so that all references to code may be made by file name and line number. Avoid duplicating material that is available elsewhere, such as the supplied datasheets; simply reference them. One of the criteria we will use in the assessment is our ability to replicate your work from the details of the submitted material. It is mandatory that all the reports (i.e. the team report and all of the individual reports) be bound together. Spiral binders and covers are available from Lab Stores or the Zepler Reception at a nominal cost. Which word processing tool you use to write the report is your choice. If you decide to use Latex you can find further details [here](https://secure.ecs.soton.ac.uk/support/textools/), and you can use ECS Forge[[4]](#footnote-4) or ECS Source Kettle[[5]](#footnote-5) to keep up to date versions of the different components and bring the report together more coherently.

The team and individual reports must be submitted electronically to the ECS Electronic Handin System and on paper to the Zepler Reception by 16:00 Friday 13th March*.* Failure to submit the formal report on time will result in [the university's standard penalty.](http://www.southampton.ac.uk/assets/imported/transforms/peripheral-block/UsefulDownloads_Download/15359ED8942444C3A172DE55B7F4D75A/Late%20Submission.pdf)

# Hints and Tips

In this section you will find some suggestions and guidelines on how to carry out this project successfully.

## Project Management

1. Appoint a team manager, not to act as a tyrant but to provide a co-ordination function. A good team manager will do slightly less hands-on design, development and construction than the rest of you, but will know what everybody is doing, how far along you are, and if there are any problems. The team manager is responsible for coordinating the activities of the team, and ensuring that deadlines are met. He, or she, should be empowered to make decisions on the priority of different tasks and to alter the team’s activities accordingly. If a team is seen to have bad management the leader will receive fewer marks than the others in the team. Alternatively, a well-managed team will earn its leader extra marks.
2. If the team is not getting along contact the academic staff as soon as possible.
3. Have regular meetings, particularly at the start to thrash out the design strategy. Try to make meetings efficient by jointly putting together an agenda so that everyone understands the purpose of the meeting and can come prepared. Let everyone make a contribution; we all have something to contribute. Identify someone to record minutes of the meeting so that a summary can be promptly circulated afterwards to state unambiguously what you agreed (or disagreed!) to do.
4. Break up the work, each to his or her best skills. You will need to work as individuals as there are too many sub-sections for working in pairs. Use a skills audit to divide up the tasks.
5. Look at the sub-systems you need and assign people according to their skills.
6. Identify the minimum requirements to get the system working and use this to prioritise tasks. Keep it simple to start with. Make sure you reach the minimum goal early in the main laboratory week. Also consider whether you can put together a working but more limited system should any one of your modules fail. Take a rapid prototyping, or spiral model, to identify risks early.
7. Use a backup and versioning tool such as ECS Forge[[6]](#footnote-6) or Source Kettle[[7]](#footnote-7) to collect your source code, schematics, results etc in a single place that everybody has access to.
8. Find a good balance between your ambition, the novelty of your project and the challenge that you take on. It is better to be under-ambitious to begin with then add more complexity later.

## Design

1. Remember that simulation is a useful tool, and it can let you do things that are impossible otherwise.
2. Reconfigurable designs that can be extended from simple systems by means of software or firmware upgrades are easier to adapt to changing requirements.
3. Assume that your design will not work first time and think carefully about how you will test and fault-find the modules independently – if you cannot, troubleshooting will become more difficult.
4. What inputs and outputs will each team member's module need, in order to interoperate with everybody else's? This interface definition will need to be continually updated and monitored, as things rarely go exactly to plan. Begin on integrating your modules as early as possible. We find that integration is make or break in D4 – teams that succeed are the ones that start integrating their modules together early.

## Troubleshooting

1. Take care of your equipment; remember ICs can be damaged by static electricity.
2. A complex circuit that does not work does not necessarily imply a complex fault.
3. Many problems of designs failing to work are associated with power supply problems, e.g. poor decoupling, no power applied, wrong voltage applied, or wrong polarity; always use the current limiter.

## Reporting

1. Use a camera, the oscilloscope’s waveform capture and the PC’s screen-grab facility, to obtain visual records of progress and achievement.
2. When you have something working get this recordedon your Design Completion Form.
3. You should aim to complete the team component of the final report soon after the build has been completed, so that you can focus on the individual components in the run up to submission.

# Contacts

If you have any queries or problems, please contact:

|  |  |
| --- | --- |
| Management Problems | Geoff Merrett ([gvm@ecs.soton.ac.uk](mailto:gvm@ecs.soton.ac.uk))  David Oakley ([do@ecs.soton.ac.uk](mailto:do@ecs.soton.ac.uk)) |
| Technical queries | Steve Gunn ([srg@ecs.soton.ac.uk](mailto:srg@ecs.soton.ac.uk))  Rob Maunder ([rm@ecs.soton.ac.uk](mailto:rm@ecs.soton.ac.uk))  Geoff Merrett ([gvm@ecs.soton.ac.uk](mailto:gvm@ecs.soton.ac.uk)) |
| Kit & Components | David Kemmish ([dk@ecs.soton.ac.uk](mailto:dk@ecs.soton.ac.uk))  Geoff Merrett ([gvm@ecs.soton.ac.uk](mailto:gvm@ecs.soton.ac.uk))  Mark Temple ([mst@ecs.soton.ac.uk](mailto:mst@ecs.soton.ac.uk)) |
| Equipment problems | Jeff Hooker ([jh1@ecs.soton.ac.uk](mailto:jh1@ecs.soton.ac.uk)) |
| Construction issues | Jeff Hooker ([jh1@ecs.soton.ac.uk](mailto:jh1@ecs.soton.ac.uk)) |

Mark all messages with the subject: “D4 Query” to ensure a prompt reply.

Staff will circulate the reply to all teams only if they feel that this is essential.

# Appendix A: Project Proposal Form

|  |  |  |  |
| --- | --- | --- | --- |
| Team letter: |  | Name of person elected as team leader: |  |

## Responsibilities

*List the responsibilities of each team member.*

|  |  |  |
| --- | --- | --- |
| Lab pair no. | Name | Design responsibility |
|  |  |  |
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## Overall Design Summary

*Give a summary of your design.* *Please make explicit exactly what you intend to build. Remember, a working design with more features would always obtain better marks. Be aware that you will be marked against what you declare in this document. YOU are setting the standard, YOU choose your goals and what you want to achieve.*

*Include a SPECIFICATION for the system you are designing.* Be ***specific***, it’s a ***specific***ation – e.g. the specification of the audio amplifier is: a gain of *x*, a bandwidth of *y*, capable of amplifying two independent audio channels, etc.

## Module Design Proposals

*Please give details of each module of your overall design. In particular, give interfacing details between your module and other parts of the system. Complete one of these pages for each module of the design (continue on an additional sheet if necessary).*

|  |  |
| --- | --- |
| Names of people involved: |  |
| Title of Module: |  |

## Cost Estimates

*Please give detailed calculations and estimates of the overall cost of your proposed design below. Take care to include person-hour estimates for your software, board production and debugging, as well as your components and consumables. You should also estimate the production cost of your final unit (you may assume a large quantity are to be produced), the market price and determine how many need to be sold to be profitable.*

## Prototyping and Construction Method

*Briefly describe your proposed method(s) of prototyping and construction, including whether you will use any surface mount packages.*

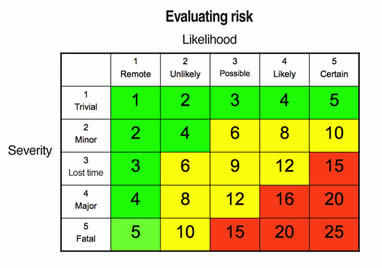
## Planned Project Activities

*Please list the activities that you intend taking place during your laboratory time, and indicate when they should occur, and who will do them. The ‘Initials’column must specify only one person. If two people are working on the same subsystem or task, you should list this as two separate activities, and be clear about what each individual is contributing to it.*

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Activity | Initials | Fri  am | Fri  pm | Mon  am | Mon  pm | Tue | Wed | Thu | Fri  am | Fri  pm | Mon  am | Mon  pm |
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## Risk Management

The D4 exercise is intensive, having demanding requirements yet running over a very short period of time. Successful project management requires management (i.e. planning) of risks. On the right hand side of this form, you should identify the predominant risks to your project, and the controls that you are going to put in place to minimise/mitigate them. Some things you may want to consider are illness of a team member(s), disruption to lab access, broken/faulty components, etc.



International Register of Certified Auditors (IRCA), “A History of Risk”, <http://www.irca.org/Global/Images/technical/inform/issue%2024/24-SAsbury-Figure1.jpg>

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **Hazard** | **Severity** | **Likelihood** | **Risk** | **Control** | **Controlled Severity** | **Controlled Likelihood** | **Controlled Risk** |
| Components are damaged/broken through misuse | 3 | 4 | 12 | Comply with ESD handling guidelines. Confirm correct wiring with datasheet before applying power. Turn off power before rewiring. Order a spare of key components, if budget permits. | 2 | 2 | 4 |
|  |  |  |  |  |  |  |  |
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# Appendix B: Kit & Component Requisition Form

You have a budget of £50 and can source additional components from the two suppliers listed below. This is over and above anything that you can obtain from within ECS. The additional suppliers have been selected due to their stock catalogue and delivery lead-time.

* Onecall (Farnell) <http://onecall.farnell.com/>
* RS <http://uk.rs-online.com/web/>

The requisition form can be found in Requisitions.xlsx from the D4 pack. If you wish to order components from both suppliers you need to complete a separate requisition form for each supplier. You should also complete a separate Requisitions Form for anything that you require from ECS stock. You will be required to hand in a hard copy of the component requisition form to David Kemmish or Mark Temple at the Lab Support Hatch by **14:00 Tuesday 24th February.** An electronic copy is also required and this should be sent to [mst@ecs.soton.ac.uk](mailto:mst@ecs.soton.ac.uk), and submitted on the ECS Electronic Handin System. *Supply of components is subject to approval of the budget holder (Geoff Merrett).*

Any use of LiPo batteries, voltages/currents in excess of the standard Risk Assessment limits must be covered by a supplementary Risk Assessment procedure ***before*** relevant components are used.

Below are example copies of the three component requisition forms. Please ensure you complete all of the required fields as failure to do so can result in late/non delivery of components. Make the description as brief as possible and supply prices exclusive of VAT. You don’t need to supply prices for components sourced from within ECS, but you should include estimates of these when you do the costing part of the project).

Most important of all is to check that the component is available and in stock.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Group:** Z | | **Project leader:** Brian Griffin | **Supplier:** Onecall | | |
| **Quantity** | **Suppliers stock code** | **Description** | **Unit price (ex. VAT)** | **Total price (ex. VAT)** | **In stock** |
| 1 | SC11597 | Blue LED | 0.25 | 0.25 | Yes |
| 3 | 3815699 | 10 way IDC socket | 0.81 | 2.43 | Yes |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Group:** Z | | **Project leader:** Brian Griffin | **Supplier:** RS | | |
| **Quantity** | **Suppliers stock code** | **Description** | **Unit price (ex. VAT)** | **Total price (ex. VAT)** | **In stock** |
| 1 | 724-8723 | ACS709 Hall Effect Sensor | 3.02 | 3.02 | Yes |
| 1 | 146-014 | Keypad | 4.92 | 4.92 | Yes |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **Group:** Z | | **Project leader:** Brian Griffin | **Supplier:** ECS | | |
| **Quantity** | **Suppliers stock code** | **Description** | **Unit price (ex. VAT)** | **Total price (ex. VAT)** | **In stock** |
| 1 |  | Stellaris Development board |  |  |  |
| ? |  | Various E12 resistors |  |  |  |
| 1 |  | Altera FPGA board + cables |  |  |  |
| 1 |  | Soldering iron |  |  |  |

# Appendix C: Class list

|  |  |
| --- | --- |
| **A**rmageddon | Presley,Samuel David |
| Casino,Andrea |
| Zaimuddin,Muhammad Arif Fikri Bin |
| Meng,Jiuxi |
| Carville,Christopher |
| Gevorkyan,Grisha |
|  |  |
| **C**loverfield | Ruttley,Nathan Edward |
| Sturgeon,Joseph Michael |
| Moore,Fiona |
| Khoja,Alaa |
| Zhi,Yubo |
| Hu,Diwen |
|  |  |
| **D**oomsday | Hayes,Harry John |
| Upton,Joshua |
| Chan,Vincent |
| Taylor,Robin |
| Chien,Samuel Haozart |
| Liu,Yushuo |
|  |  |
| **G**odzilla | Fletcher,Benjamin James |
| Rowland,Aaron |
| Karatziolas,Georgios |
| Johnson,Ryan |
| Malik,Rohan |
|  |  |
| **H**alo | Middleton-Jones,James |
| Wilson,Henry Walter |
| Patel,Rinesh |
| Barber,Terra |
| Zeng,Junming |
| Lan,Tu |
|  |  |
| **I**ndependence | Borisevic,Artur |
| Sheppard,Gerry |
| Lau,Anthony Hok Bun |
| Aggarwal,Sumit |
| Hamlin,Peter |
| Shao,Shuai |
|  |  |
| **M**atrix | Cosslett,Jack |
| Maskell,Dominic |
| Harris,Kieran James |
| Hurst,Oliver Sebastian |
| Bengougam,Michael |
|  |  |
| **O**blivion | Eyre,Patrick |
| Percival,Huw |
| Akurunwa,Chidi David |
| Clark,Thomas James |
| Fok,Tobias Tak Jing |
| Sun,Jiayang |
|  |  |
| **P**rometheus | Curati-Alasonatti,Emma Clotilde |
| Scheul,Tudor Emilian |
| Niven,Jonathan Gregory |
| Thomas,Katrina |
| Holbrow,Christopher Iain |
|  |  |
| **R**obocop | Saxby,Robert |
| Gonzalez,Nicholas |
| Scott-South,Michael |
| Woodward,Ciaran |
| Bashaagha,Ali Fathi Ali |
| Zhou,Fuxin |
|  |  |
| **T**erminator | Khorani,Edris  Agu,Kenechukwu Richard  Chahal,Hardeep Singh  Furlong,Timothy James  Mahendra Jain,Shantanu |

# Appendix D: Design Completion Form

*To be completed by the lab supervisor during the time in the lab to record milestones.* ***This form is an example and you MUST edit it to identify your own milestones*** *(10-15) that you will attempt to meet during the progression of your design. Think about MILESTONES (what you’ll show/deliver) rather than TASKS (what you’ll do). You should aim to have a few milestones per subsystem (which probably build on each other), plus a couple of system milestones reflecting system integration. A single copy of this form should be printed, on one sheet of Landscape A4 paper, and brought to each lab session. It will be finalised by 17:00, on Monday 09th March.*

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| Component of system/Milestone | Supervisor | Time/Date | Comments (all/part/none working; protoboard/constructed) | | | |
| Wireless modules interfaced with embedded devices |  |  | Data rate \_\_\_\_\_\_ kbps | | | |
| Wireless communication of speech between devices |  |  | Audio bandwidth \_\_\_\_\_\_ Hz -> \_\_\_\_\_\_ kHz, Typical range \_\_\_\_\_\_ m | | | |
| Bi-Directional Voice communication between devices |  |  | Latency \_\_\_\_\_\_ ms | | | |
| Offline encryption/decryption of data on embedded device |  |  |  | | | |
| Encryption/decryption of transmitted audio |  |  |  | | | |
| Encryption/decryption of transmitted messages |  |  |  | | | |
| Sinusoidal input to audio amplifier can drive 8 Ω load |  |  | Gain \_\_\_\_\_ Bandwidth \_\_\_\_\_ Hz -> \_\_\_\_\_ kHz | | | |
| Amplifier driving speaker with volume control |  |  |  | | | |
| Interfacing of LCD with processor to present basic GUI |  |  |  | | | |
| Data messages entered via keypad |  |  |  | | | |
| Data messages transmitted, received and displayed on LCD |  |  |  | | | |
| Peer-to-peer transmission of messages via a third device |  |  |  | | | |
| Processor can record FAT formatted wav files to SD card |  |  |  | | | |
| Processor can replay audio recordings from SD card |  |  |  | | | |
| Power management of complete system |  |  | \_\_\_\_\_ mA , at \_\_\_\_\_ V = \_\_\_\_\_\_ mW. Batteries should last for \_\_\_\_\_ hrs. | | | |
| Complete system is integrated |  |  | Mass \_\_\_\_\_\_ g (per device), Dimensions \_\_\_\_\_ x \_\_\_\_\_ x \_\_\_\_\_ | | | |
| Milestones finalised by supervisor: | ……………………………………………… Signed ………………………………………………………… Date | | |  |  |
| Prototype hardware handed over to: | ……………………………………………… Signed ………………………………………………………… Date | | |  |  |
| Other items returned to Lab support hatch and checked by: | ……………………………………………… Signed ………………………………………………………… Date | | |  |  |

# Appendix E: Project Completion Form

## Cost Estimates

*Please give detailed calculations and estimates of the overall cost of your actual design below. Take care to include person-hour estimates for your software, board production and debugging, as well as your components and consumables. You should also estimate the production cost of your final unit (you may assume a large quantity are to be produced), the market price and determine how many need to be sold to be profitable. Account for any differences between the actual values and the values given in your original project proposal form.*

## Design Changes

*Briefly summarise any design changes your team had to make to the original design proposal, in order to get your system to work. Do not go into vast detail, as it is anticipated that this will be done by the individuals responsible for these components of the design in the formal report.*

## Actual Project Activities

*Please list the activities that took place during your laboratory time, and indicate when they occurred, and who did them. The ‘Initials’column must specify only one person. If two people worked on the same subsystem or task, you should list this as two separate activities, and be clear about what each individual contributed.*

|  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Activity | Initials | Fri  am | Fri  pm | Mon  am | Mon  pm | Tue | Wed | Thu | Fri  am | Fri  pm | Mon  am | Mon  pm |
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## Discrepancy in Project Activities

*Comment on any major differences between the planned and actual project activities.*

## Assessment of Effort

*The table below will be used as an indication how team marks should be allocated across the team.*

|  |  |  |
| --- | --- | --- |
| Name | Signature | % of effort |
|  |  |  |
|  |  |  |
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*If the breakdown is not equal please provide a short explanation below:*

# Appendix F: Box of Bits

|  |  |
| --- | --- |
| Qty | Item |
| 2 | [Il Matto AVR prototyping board](https://secure.ecs.soton.ac.uk/notes/ellabs/1/x2/) kit |
| 1 | Il Matto SD card adaptor |
| 2 | [RFM12B-S2 Wireless Transceivers with Breakout Boards](http://www.hobbytronics.co.uk/rfm12b-wireless-breakout) |
| 1 | [SD card](http://onecall.farnell.com/transcend/ts2gsdc/card-sd-2gb/dp/2290235) |
| 1 | [Il Bagatto CPLD prototyping board](https://secure.ecs.soton.ac.uk/notes/elec2032/D4/Micro%20Arcana/) kit |
| 1 | [AVR Dragon](http://www.atmel.com/tools/avrdragon.aspx) |
| 1 | [10 way JTAG program/debug cable](http://onecall.farnell.com/molex/92321-1020/cable-assembly-ribbon-10way-20cm/dp/1012209) |
| 2 | [Paired X-Bee Modules](https://secure.ecs.soton.ac.uk/notes/elec2032/D4/XBee/) |
|  | Connectors and cables |

# Appendix G: Design Clinic Schedule

The schedule for the clinic on Monday 23rd February is given below. Each slot is only for 20 minutes, so come prepared. Please arrive promptly and wait outside the electronic laboratory until your slot. Tim Forcer will be holding the clinic and he will be in the D area of the laboratory. This is the only time you are permitted in this laboratory on this day; you are free to use the computers and printers on Level 3 if you desire.

|  |  |
| --- | --- |
| Team | Time |
| Armageddon | 11:00 – 11:20 |
| Cloverfield | 11:25 – 11:45 |
| Doomsday | 11:50 – 12:10 |
| Godzilla | 12:15 – 12:35 |
| Halo | 12:40 – 13:00 |
| Independence | 14:00 – 14:20 |
| Matrix | 14:25 – 14:45 |
| Oblivion | 14:50 – 15:10 |
| Prometheus | 15:15 – 15:35 |
| Robocop | 15:40 – 16:00 |
| Terminator | 16:00 – 16:20 |

# Appendix H: Bench Allocation

Each team is allocated a set of three benches for their use throughout D4, plus an additional bench that they can use for half a day (as specified by am/pm below). With the exception of these half-day benches (which must clear at the end of the morning/afternoon), you can leave your work on your benches throughout D4 – there is no need to clear away over lunch or at the end of the day. Therefore, for fairness and for the protection of other teams’ work, you MUST only use benches that are assigned to your team.



# Appendix I: Check List

## Week 0: Introduction

|  |  |
| --- | --- |
|  | Attend Kick-off presentation (Thursday 19th February) |
|  | Team Meeting and appoint Team Leader (Thursday 19th February) |
|  | Read this document (Thursday 19th February) |
|  | Meet to discuss and prepare initial design (Friday 20th February) |

## Week 1: Design, investigation and simulation

|  |  |
| --- | --- |
|  | Collect Box of Bits from the Lab Support Hatch (Monday 23rd February) |
|  | Attend Design Clinic (Monday 23rd February) |
|  | Prepare Detailed design (Monday – Thursday) |
|  | Submit Kit & Component Requisition From (Deadline: 14:00, Tuesday 24th February) |
|  | Submit Project Proposal Form (Deadline: 10:00, Friday 27th February) |
|  | First 3 hour lab session for feedback, simulation and prototyping (Friday 27th February) |
|  | Negotiate Design Completion Form with Geoff, Steve or Rob. |

## Week 2: Prototyping and construction

|  |  |
| --- | --- |
|  | Second 3 hour lab session for feedback, simulation and prototyping (Monday 2nd March) |
|  | Lab open for some time each day, but no supervision - limited support (Tuesday – Thursday) |
|  | 6 hours in lab (Friday 6th March) |

## Week 3: Final assembly, evaluation, presentation and report production

|  |  |
| --- | --- |
|  | 6 hours in lab - complete system integration and final testing (Deadline for construction: 16:30, Monday 09th March) |
|  | Capture still imagery and video footage of your prototype in action (Monday) |
|  | Finalise Design Completion Form (Deadline: 17:00, Monday 09th March) |
|  | Complete Project Completion Form |
|  | Complete team component of final report |
|  | Write individual reports |
|  | Combine & Submit Final Report (Deadline: 16:00, Friday 13th March) |

## Week 4: Trade fair

|  |  |
| --- | --- |
|  | Prepare presentation slides and video advert |
|  | Submit presentation and video advert (Deadline: 12:00, Thursday 19th March) |
|  | Everybody attends Trade Fair (44/1041, Friday 20th March, 10:00 – 13:00) |
|  | One team member presents at the Trade Fair |
|  | One team member attends demonstrations (Lab, Friday 20th March, 14:00 – 17:00) |
|  | Everybody attends Closing Ceremony (Lab, Friday 20th March, 17:00 – 18:00) |

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2. There is no obligation to use any of the items in the “box of bits”. [↑](#footnote-ref-2)
3. We will endeavour to acquire these as soon as possible, but remember that this will depend on the suppliers’ stock and the external and internal postal services. You should plan to receive your kit at midday on Tuesday 3rd of March. [↑](#footnote-ref-3)
4. <http://forge.ecs.soton.ac.uk> [↑](#footnote-ref-4)
5. <http://sourcekettle.ecs.soton.ac.uk/> [↑](#footnote-ref-5)
6. <http://forge.ecs.soton.ac.uk> [↑](#footnote-ref-6)
7. <http://sourcekettle.ecs.soton.ac.uk/> [↑](#footnote-ref-7)